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Dielectric surface-polarity tuning and enhanced operation stability of solution-processed organic field-effect transistors

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ABSTRACT

The electrical performance of triethylsilylethynyl anthradithiophene (TES-ADT) organic field-effect transistors (OFETs) was significantly affected by dielectric surface polarity controlled by grafting hexamethyldisilazane and dimethyl chlorosilane-terminated polystyrene (PS-Si$(CH_3)_2$Cl) to 300-nm-thick SiO_2 dielectrics. On the untreated and treated SiO_2 dielectrics, solvent–vapor annealed TES-ADT films contained millimeter-sized crystals with low grain boundaries (GBs). The operation and bias stability of OFETs containing similar crystalline structures of TES-ADT could be significantly increased with a decrease in dielectric surface polarity. Among dielectrics with similar capacitances (10.5–11 nF cm^{-2}) and surface roughnesses (0.40–0.44 nm), the TES-ADT/PS-grafted dielectric interface contained the fewest trap sites and therefore the OFET produced using it had low-voltage operation and a charge-carrier mobility ~1.32 cm^2 V^{-1} s^{-1}, on–off current ratio >10^6, threshold voltage ~0 V, and long-term operation stability under negative bias stress.

1. Introduction

Organic field-effect transistors (OFETs) may enable remarkable advances in emerging technologies such as flexible displays, sensors, and radio frequency identification (RFID) tags [1–3]. However, OFETs used as components in commercial products should be capable of reliable operation at low voltages for prolonged periods of time so that they can be driven using small batteries or solar energy [4,5].

Many localized traps have been observed in organic semiconductor films or at the semiconductor/dielectric interfaces in OFETs [5–7]. The localized traps are caused by structural properties of organic semiconductors, such as crystalline defects and grain boundaries (GBs), and by polar dielectric functionalities at the interface. The traps cause reduced charge carrier mobility (μ_{FET}) or large threshold voltages (V_{th}) in OFETs [5,8]. Most studies conducted to date have focused on solving these problems, and have led to development of novel organic semiconductors and dielectric materials, and to semiconductor/dielectric interface engineering methods [7–9].

The electrochemical nature of the active moieties on dielectric surfaces has an important influence on the formation of interface traps, and consequently also on modulation of the number of charge carriers in the channel [10–13]. Among such functional groups located at the

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organic semiconductor and dielectric interface, highly polar groups such as hydroxyl influence μ_{FET} and device instability, which is induced by deep localized trap states [6,10–13]. Before OFETs can be commercialized as driving components in display backplanes or logic circuitry in RFID tags, the OFETs must have good operational stability [11].

In this work, we introduced organic layer to optimize the dielectric surface properties to achieve solution-processed OFETs with high electrical performance and long-term operational reliability. Solution-processed triethylsilylethynyl anthradithiophene (TES-ADT) films were then fabricated on untreated (bare) and ultrathin organic layer-grafted SiO_2 dielectrics. On the physicochemically stable dielectrics, simple solvent–vapor annealing was used to produce spin-cast TES-ADT films containing millimeter-sized crystals, which enabled minimization of the effects of GB-related trap sites on the electrical performance of OFETs. The electrical performance of all OFETs and the dielectric surface polarity-dependent bias stability were characterized after applying gate-bias stress for up to 12 h. Based on the variations in threshold voltage (V_{th}), the trap information was clarified using a stretched exponential equation [14]. Additionally, the density of states (DOS) of the traps in the band gap was determined using photo-excited charge-collection spectroscopy (PECCS).

2. Experimental

2.1. Materials and sample preparation

Highly-doped n-type (1 0 0) Si wafers with 300-nm-thick thermally-grown SiO_2 layers were used as gate substrates. Hexamethyldisilazane (HMDS, Aldrich) and dimethyl chlorosilane-terminated polystyrene (PS-Si$(CH_3)_2$Cl, M_w = 8000, PDI = 1.06, Polymer Source) as the surface modification layer were used without further purification. To fabricate surface-functionalized oxide dielectrics, the substrates were first cleaned by organic solvent treatment (acetone) and UV-ozone exposure. PS-Si$(CH_3)_2$Cl was dissolved (0.5 wt%) in toluene, and the solutions were stirred in an N_2-purged glove box (H_2O and O_2 <0.1 ppm). HMDS was used as master solution without any dilution. All solutions were spin-coated onto substrates in ambient air, and resulting films were annealed 120 °C for 30 min. The layers were annealed at 110 °C for 60 min, then sonicated in a toluene bath for 3 min to remove the ungrafted HMDS and PS-Si$(CH_3)_2$Cl residues. TES-ADT films were spin-cast onto the bare SiO_2, HMDS-, and PS-grafted SiO_2 dielectrics from 1,2-dicholoroethane (DCE, Aldrich) solution, then further solvent for 15–20 min annealed in a closed jar containing DCE vapor. The resulting film thickness of TES-ADT was 55 ± 2 nm, characterize using an elipsometer (J.A. Woollam Co., Inc.). Finally, top-contact Au electrodes on the TES-ADT films were thermally evaporated through a shadow mask (channel length L = 100 μm; width W = 1500 μm).

2.2. Characterization

Capacitance (C_i) values of the dielectrics, which were sandwiched between Au dots and highly doped n-type (1 0 0) Si substrates, were measured using an Agilent 4284 Precision LCR Meter. Electrical characterization of TES-ADT OFETs was performed using a Keithley 4200 SCS at room temperature in an N_2-purged glove box. The resulting μ_{FET} values were calculated as $I_D = \mu_{FET}C_iW(2L)^{-1}(V_G - V_{th})^2$ where V_G is gate voltage.

Surface energies (γ_s) of the dielectrics were characterized by measuring the contact angles (θ) of two liquid droplets (water and diiodomethane) on the substrates in a contact angle measurement system (SEO300A, SEO). The γ_s values were calculated using the following equation [15]:

$$1 + \cos\theta = \frac{2(\gamma_s^d)^{0.5}(\gamma_{lv}^d)^{0.5}}{\gamma_{lv}} + \frac{2(\gamma_s^p)^{0.5}(\gamma_{lv}^p)^{0.5}}{\gamma_{lv}}, \quad (1)$$

where γ_{lv} is the surface energy of the test liquid and superscripts d and p refer to the dispersive and polar components, respectively.

Surface morphologies of TES-ADT films were measured using an atomic force microscope (VEECO Dimension 3100, VEECO) and a polarized optical microscope (Axiophot El-Einsatz, Carl Zeiss Microscopy). A 2D grazing X-ray diffraction (GIXD) experiment was performed at the 3C and 9A beamlines of the Pohang Accelerator Laboratory (PAL), Korea.

Photo-excited charge-collection spectroscopy (PECCS) was set up in a dark box containing a 500 W Hg(Xe) arc lamp light source, a grating monochromator covering a spectral range of 254–1000 nm wavelength, an optical fiber (diameter: 200 μm), and a semiconductor parameter analyzer (HP 4155C). The OFETs were exposed to selected photons with wavelength that descended stepwise from 1000 nm, and ΔV_{th} was then extracted from the photo-induced transfer curves of the OFETs.

3. Results and discussion

Fig. 1 shows a top-contact electrode OFETs containing TES-ADT film on bare and 300-nm-thick SiO_2 dielectrics treated with either PS-Si$(CH_3)_2$Cl or HMDS. PS-Si$(CH_3)_2$Cl could be grafted to the SiO_2 dielectrics by chemical coupling between the end-functional groups and silanol (the surface hydroxyl group on SiO_2), resulting in the formation of a 4–6 nm-thick layer (referred to as PS brush) [11], which is much thicker than a typical HMDS layer (<1 nm). These ultrathin organic layers imparted the resulting bilayer SiO_2 dielectrics with $C_i \approx 10.5$ nF cm^{-2} (PS brush) and ≈10.7 nF cm^{-2} (HMDS) at 1 kHz, which are comparable to those of bare SiO_2 (11 nF cm^{-2}). In addition, all dielectric systems had low surface roughness ranging from 0.40 to 0.44 nm (Table 1), characterized from their surface morphologies (Fig. S1). The surface polarities (χ_p) of the dielectric systems were 0.01 (PS brush), 0.34 (HMDS), and 0.46 (bare) based on the ratios of polar components (γ^p) to the total surface energy (γ) (Table 1). The surface polar components are attributed to polar interactions arising from permanent or induced dipoles, and to hydrogen-bonding involving the highly polar surface functional groups. In our system, silanol (Si-OH) on the bare SiO_2 dielectric is the main contributor to χ_p, while decreased

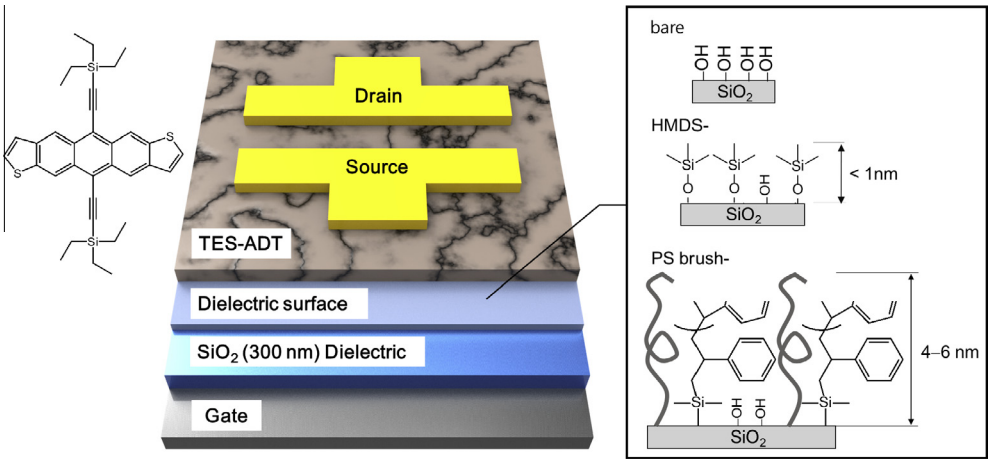

Fig. 1. Schematic diagram of a top-contacted Au electrode OFET containing TES-ADT film on three different dielectric surfaces. (PS brushes were elongated vertically, but not ordered.)

Table 1
Characteristics of dielectrics used in this study.

Dielectric	Capacitance (nF cm^{-2})	Surface roughness (nm)	Surface energy (mJ m^{-2})			Polarity
			γ_s^p	γ_s^d	$\gamma = \gamma_s^p + \gamma_s^d$	$\chi_p = \gamma_s^p/\gamma_s$
Bare SiO_2	11.0	0.40 ± 0.03	26.34	30.03	56.37	0.46
HMDS-SiO_2	10.7	0.42 ±0.05	14.91	28.71	43.62	0.34
PS brush-SiO_2	10.5	0.44 ±0.04	0.48	39.05	39.53	0.01

with an increase in thickness of the organic buffer layers grafted to the SiO_2 surface. As a result, the 4–6 nm thick PS brush layer provided almost full passivation of silanol on the dielectric surface, comparable to that of the bulk PS film [11].

TES-ADT films (50 nm thick) were spin-cast onto these gate dielectrics, and millimeter-sized crystals developed in the films after DCE solvent annealing, resulting in the lateral sizes of TES-ADT crystals becoming greater than those of the channel (Fig. 2(a)–(c)). As shown in Fig. 2(d)–(f), the DCE-annealed TES-ADT films showed typical layer-by-layer stacked crystal morphologies [16,17]. Additionally, the 2D GIXD patterns of these TES-ADT films confirmed that the multiple-layered crystals were preferentially oriented with an "*edge-on*" molecular conformation on all of the dielectric surfaces (Fig. 3). Regardless of the dielectric surface polarity, the 2D GIXD patterns showed highly ordered and intense X-ray reflection peaks of (00*l*) and {*hk*} planes along the Q_z (out-of-plane) and Q_{xy} (in-plane) axes, respectively, corresponding to 3D layered crystals with a triclinic unit cell [16–18].

The electrical performance and stabilities of the resulting OFETs were not expected to differ greatly from each other owing to the similar crystal structures, which contained highly ordered crystals with fewer lateral GBs (as charge transport barriers) [19–21]. Crystalline GBs do not significantly affect device stability under gate-bias stress [22–24], but further minimization is still required to achieve high performance OFETs.

Fig. 4(a) shows typical drain current–gate voltage (I_D–V_G) transfer curves of a top-contact Au electrode TES-ADT OFETs operated in a V_G range of 5 to −5 V in the saturation regime (drain voltage V_D = −5 V). The electrical properties of all OFETs are summarized in Table 2. For all devices, the off-currents of I_D could be maintained at a few picoamperes. The maximum I_D of the PS brush-SiO_2 system was approximately one order of magnitude higher than those of the other systems, producing current on/off ratios greater than 10^6. The μ_{FET} decreased with increasing dielectric surface polarity, with values of 1.32 cm^2 V^{-1} s^{-1} (PS brush), 0.27 cm^2 V^{-1} s^{-1} (HMDS), and 0.07 cm^2 V^{-1} s^{-1} (bare) being observed. The PS brush-SiO_2 system showed a much smaller subthreshold slope (*SS*) 0.20 V decade^{-1} than other systems. *SS* is defined as the amount of change in V_G required to produce a 10 times change in I_D, is an index for the slope of the transfer curve in the subthreshold regime [25]. In particular, the *SS* of our device with PS brush-SiO_2 was just three times higher than that (0.060 V decade^{-1}) of single-crystal Si FET at room temperature, and is comparable to those of the several OFETs that use high C_i dielectrics [4,5,26]. V_G-induced charge carriers in the subthreshold regime were influenced significantly by the charge trapping at the interface [27]. Therefore, the observation that of the PS brush-treated SiO_2 system had the smallest *SS* strongly suggests that the surface-grafted PS layer with a film thickness of 4–6 nm can deactivate the silanol residue on the SiO_2 surface as trap sites more effective than can the HMDS layer (<1 nm).

The device hysteresis (i.e., the difference between transfer curves obtained by sweeping in the off-to-on and on-to-off directions) was similar to the variation trend in μ_{FET}. The PS brush-treated SiO_2 produced the least hysteresis

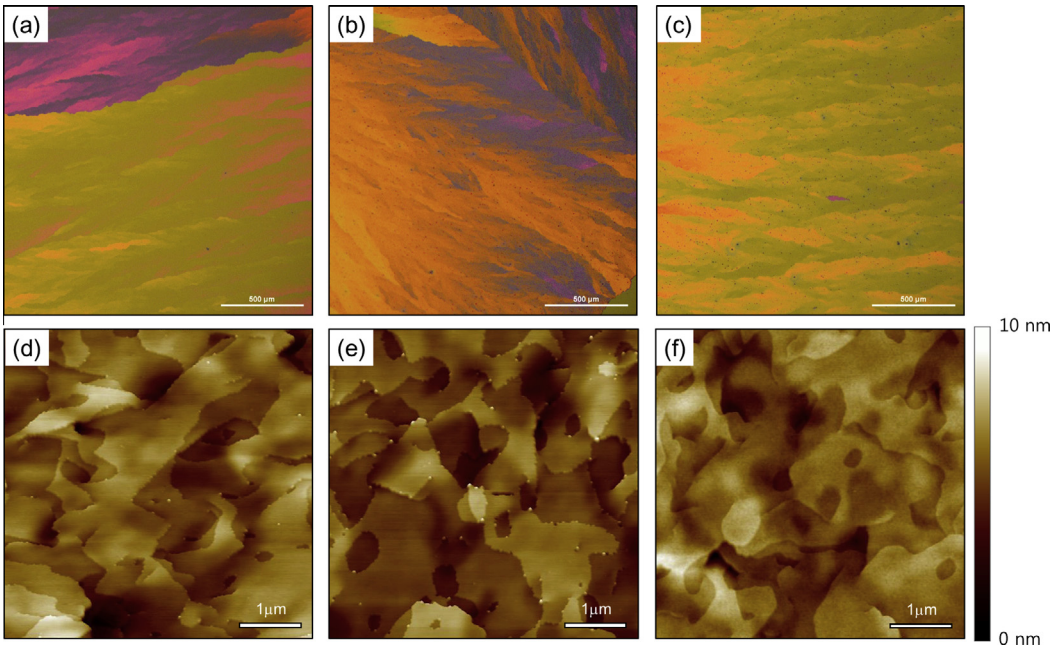

Fig. 2. Optical microscopic images and AFM topographies of TES-ADT films on (a and d) bare, (b and e) HMDS-, and (c and f) PS brush-SiO_2 dielectrics, respectively.

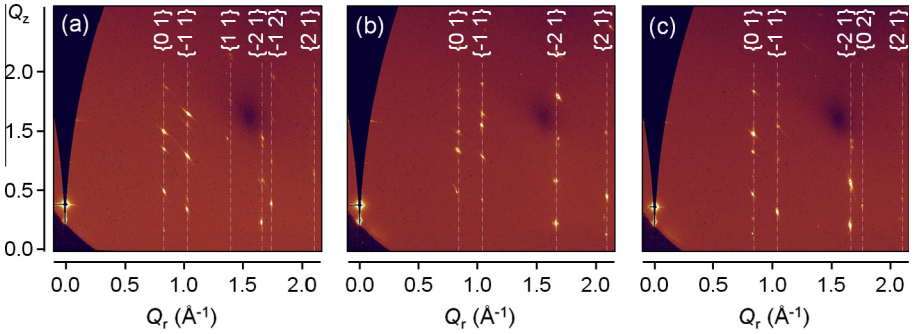

Fig. 3. 2D GIXD patterns of TES-ADT films on (a) bare, (b) HMDS-, and (c) PS brush-SiO_2 dielectrics, respectively. (The lateral sizes of TES-ADT crystal grains were much bigger than that (width × height = 200 μm × 50 μm) of the X-ray beam; therefore some of the crystal diffractions were missed depending on the local orientation of the TES-ADT crystals.)

(Fig. 4(a)). The TES-ADT films showed similar crystal structures on the three different dielectric surfaces, so the hysteresis must be related mainly to the trap sites at the semiconductor/dielectric interface (originating from the existence of polar groups, e.g., silanol at the SiO_2 surface) [27,28].

The long-term bias stability of all TES-ADT OFETs was investigated by measuring V_{th} as a function of time (t_{bias}) under an applied gate-bias stress of −5 V for up to 12 h. Fig. 5 represents bias stability of the TES-ADT OFETs was dependent on the dielectric surface polarity. As expected, the OFET on the PS brush-treated SiO_2 dielectric showed outstanding bias stability. Specifically, the variation in V_{th} (ΔV_{th}) was only −0.3 V even after t_{bias} = 12 h (Fig. 5(c)). In contrast, OFETs on bare and HMDS-treated SiO_2 dielectrics showed $\Delta V_{th} \sim -4$ V (Fig. 5(a) and (b)).

The t_{bias}-dependent ΔV_{th} (Fig. 6(a)) suggests that non-polar PS grafting to the SiO_2 surface should effectively suppress interface charge-trapping. Grafting density is generally smaller in polymers than in oligomeric self-assembled monolayers, but *ML* thick layers formed by the grafted polymers enable silanol residue to be separated from the semiconductor/dielectric interface. This argument could be clarified by modeling ΔV_{th} using a stretched exponential equation [14]:

$$\frac{V_{th} - V_{th,i}}{V_G - V_{th,i}} = 1 - \frac{1}{\{1 + \exp[(E_{th} - E_A)/k_B T_o]\}^{1/(\alpha-1)}}, \quad (2)$$

where $V_{th,i}$ is the initial V_{th} at t_{bias} = 0, E_A is a typical activation energy for trap creation, $k_B T_0$ is the slope of the activation energy distribution, α is a constant,

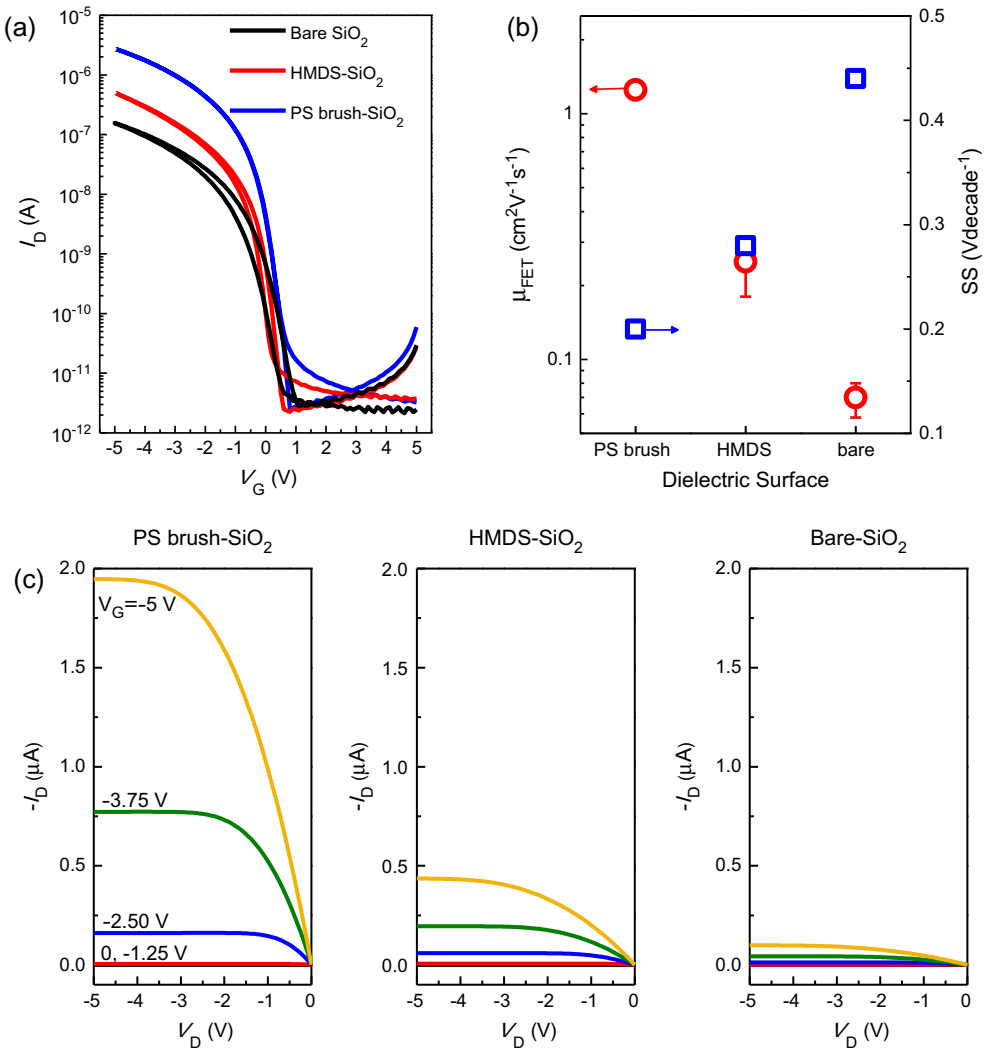

Fig. 4. (a) Transfer curves of the TES-ADT OFETs employing bare, HMDS-, and PS brush-treated SiO_2 dielectrics (V_D = −5 V), and (b) the corresponding μ_{FET} and *SS* values. (c) Output curves of the TES-ADT OFETs employing bare, HMDS-, and PS brush-treated SiO_2 dielectrics.

Table 2
Electrical properties, E_A, and k_BT_0 of TES-ADT-based OFETs on bare, HMDS-, and PS brush-treated SiO_2 surfaces.

Dielectric	μ_{FET} ($cm^2\ V^{-1}\ s^{-1}$)	V_{th} (V)	I_{on}/I_{off}	*SS* (V decade^{-1})	E_A (eV)	k_BT_0 (eV)
Bare SiO_2	0.07 ± 0.01	−0.138	1.16×10^5	0.44	0.524	0.027
HMDS-SiO_2	0.27 ± 0.07	−0.635	1.43×10^5	0.28	0.571	0.034
PS brush-SiO_2	1.32 ± 0.05	−0.062	1.02×10^6	0.20	0.775	0.048

$E_{th} = k_BTln(\nu t)$ corresponds to the thermalization energy, k_B is the Boltzmann constant, T is the temperature and ν is the attempt-to-escape frequency. The fitting parameters ν and α were selected as 10^5 Hz and 1.5 respectively, as determined for TES-ADT in a previous study [18,29].

First, the parameters E_A and k_BT_0 in (2) were selected to match fitting curves (Fig. 6(b), solid lines) with the experimental $\Delta V_{th}/\Delta V_0$ (Table 2). The resulting E_A values of PS brush-, HMDS-, and bare SiO_2 systems were 0.775 eV, 0.571 eV, and 0.524 eV, respectively. The TES-ADT/PS brush interface had the highest energy barrier to generate charge traps, and this high barrier is the source of the high device performance and stability of the TES-ADT OFETs.

To investigate the nature of the interface traps and their distributions in the TES-ADT OFETs, photo-excited charge-collection spectroscopy (PECCS) was conducted for the same batch devices used in the *I–V* characterization. The basic principles and experimental details of the PECCS have been described elsewhere [30]. Fig. 7(a) shows a schematic diagram of the optically probing PECCS set-up, the

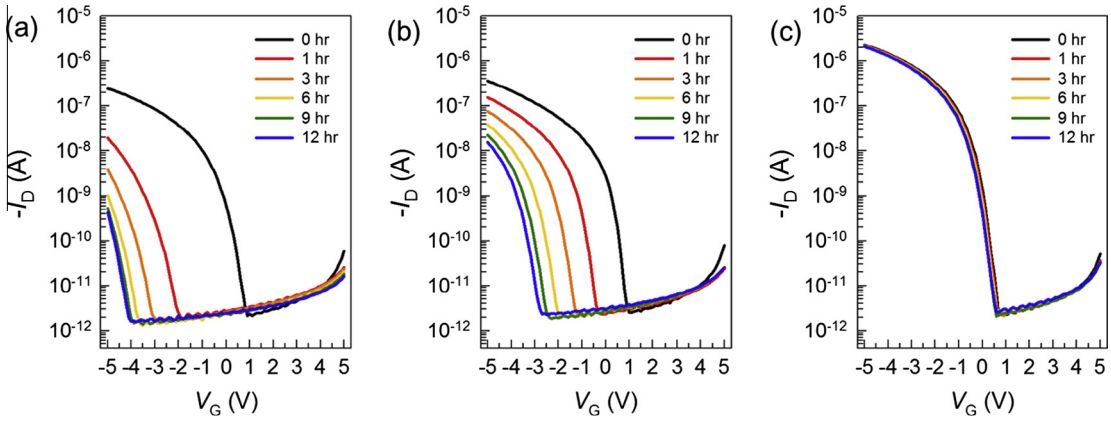

Fig. 5. I_D–V_G transfer curves of TES-ADT OFETs on (a) bare, (b) HMDS-, and (c) PS brush-SiO_2 dielectrics, depending on t_{bias} under an applied gate bias stress of −5 V (V_D = 0 V).

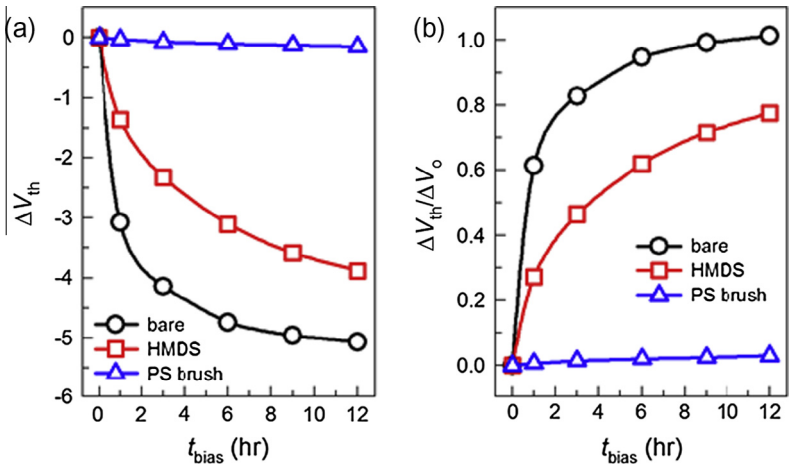

Fig. 6. (a) t_{bias}-dependent ΔV_{th} and $\Delta V_{th}/\Delta V_o$ in the TES-ADT OFETs based on bare, HMDS-, and PS brush-SiO_2 dielectrics. (In (b), the solid curves were fitted using Eq. (2).)

photo-induced V_{th} of a working device is extracted by using a monochromatic photon beam to liberate charges trapped at the interface, and ΔV_{th} was used to characterize the density of states (DOS) of the interface traps [30,31]. Fig. 7(b) shows the DOS vs. photon energy profiles extracted from the operating TES-ADT OFETs on the three different types of dielectric surfaces. Comparison of these profiles with the optical absorbance spectrum of a TES-ADT film on the PS brush-SiO_2 dielectric indicating the optical band gap at E = 1.89 eV (see the green line and the blue arrow-marked position in Fig. 7(b)) revealed that PECCS could indicate DOS below 2.04 eV (e.g. 1.55, 1.70, and 1.96 eV); therefore, PECCS is a sensitive tool to investigate the distribution of interface traps. In the PECCS profiles of the TES-ADT films, the energy state at 2.04 eV (marked by the red arrow) corresponded to the band gap energy between the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) [32]; this correspondence suggests that in the PECCS profiles the intense DOS profiles below the HOMO–LUMO band gap are related to the trap states within the band gap.

The DOS of the traps within the HOMO–LUMO band gap were highly dependent on the dielectric surface polarity (Fig. 7(b)). The portions and distributions of the interface traps appeared to decrease in magnitude as surface polarity decreased. For the PS brush-SiO_2 system, all DOS values at E = 1.55, 1.70, and 1.96 eV were below 5×10^{11} cm^{-2} eV^{-1}, and were approximately one order of magnitude smaller than those for the other samples. The bias-induced ΔV_{th} and PECCS results indicate the surface hydroxyl groups on the dielectrics might act as the main trap sites for the charge carriers, and that the PS-brush layer can effectively reduce the large numbers of these traps, resulting in the low-V operation and high electrical performance of TES-ADT OFETs (μ_{FET} = 1.32 cm^2 V^{-1} s^{-1}, SS = 0.2 V decade^{-1}, $V_{th} \sim 0$ V), which remained almost unchanged after negative bias stress for 12 h.

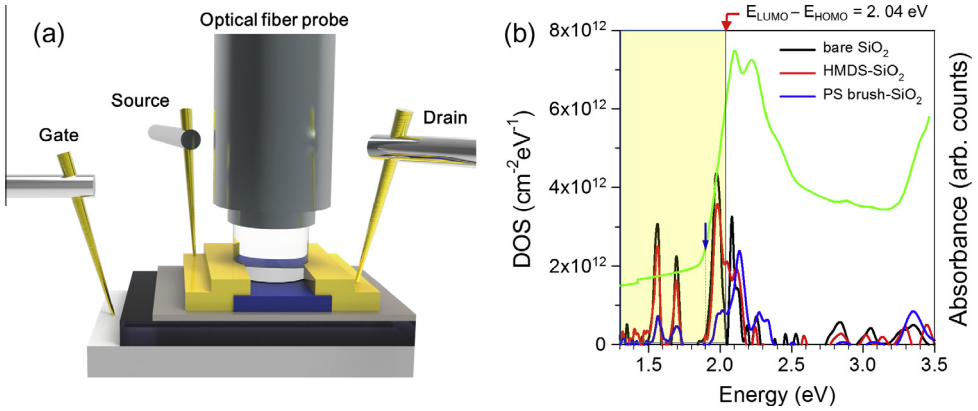

Fig. 7. (a) Schematic diagram of an optical probing set-up for the PECCS analysis. (b) DOS profiles of the TES-ADT OFETs based on bare, HMDS-, and PS brush- SiO_2 dielectrics. The optical absorbance spectrum of a DCE-annealed TES-ADT films on a quartz glass substrate (green curve). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

4. Conclusion

We demonstrated an enhanced interface system for high performance and long-term stable TES-ADT OFETs. We also investigated the correlations among the surface polarities of the dielectrics, interface trap formation, and corresponding device performances by conducting several OFET characterizations, including simple transistor measurements, gate-bias stress measurements, and PECCS. The introduction of a non-polar PS brush layer onto SiO_2 reduced the number interface traps compared to other relatively polar dielectrics; this reduction is the main factor that contributes to the high electrical performance with $\mu_{FET} \sim 1.32\ cm^2\ V^{-1}\ s^{-1}$, on–off current ratio $>10^6$, and $V_{th} \sim 0$ V, as well as to its excellent stability under sustained gate-bias stress.

Acknowledgments

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Appendix A. Supplementary material

Supplementary material associated with this article can be found, in the online version, at http://dx.doi.org/10.1016/j.orgel.2014.11.022.

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