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Effect of Al incorporation on the performance and reliability of p-type metal-oxide-semiconductor field effect transistors

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ABSTRACT

This study examined the performance and reliability of HfO_2 gate dielectrics in p-type metal-oxide-semiconductor field effect transistors (pMOSFETs) capped with Al or Al_2O_3. The presence of Al capping deteriorated the pMOSFET scalability and channel mobility compared to Al_2O_3 capping. Al capping caused a higher rate of Al diffusion in the HfO_2 dielectric layer, reducing the device performance and oxide thickness scaling. This degradation of the negative bias temperature instability of the Al-incorporated sample was attributed to decay of the interface quality rather than to a decrease in charge trapping in the bulk high-*k* dielectric.

1. Introduction

The scaling down of metal-oxide-semiconductor field effect transistors (MOSFETs) through the gate-last integration of high-*k* dielectrics and metal electrodes in the gate stacks for high-performance logic devices [1,2] can extend the lifetime of planar complementary metal-oxide-semiconductors (CMOS). Nevertheless, low threshold voltages (V_{th}) for *n*-type MOSFETs (nMOSFETs) and p-type MOSFETs (pMOSFETs) have only been achieved through low temperature processing [3,4]. Gate electrodes require further research to maintain the appropriate effective work function (EWF) after high-temperature processing (>1000 °C) to allow a simpler integration processes. The deposition of capping materials on high-k dielectrics might be one of best ways of achieving the optimum effective work function suitable for both nMOSFETs and pMOSFETs (4.1–4.3 eV and 5.0–5.2 eV, respectively) [5,6]. The incorporation of rare earth elements, such as La [7-9], Gd [10,11], Er [12] or Sc [13], in gate dielectrics has been reported to be effective in reducing the work function of nMOSFETs.

A large number of elementary and binary metals have been investigated to obtain a desirable V_{th} (-0.2 V to -0.3 V) for pMOSFETs with an equivalent oxide thicknesses (EOT) under 1 nm. On the other hand, obtaining metal gate electrodes with a sufficiently high work function for pMOSFETs is difficult due to "work function roll-off phenomena" [14-16]. Among the many possible approaches, the incorporation of aluminum into dielectrics has attracted considerable attention because it can positively shift the flatband voltage of MOSFETs [15,17]. The mechanism of the EWF shift in both n and pMOSFETs involves the formation of dipoles in the dielectric stack [15,18-22]. On the other hand, Al incorporation has disadvantages in scaling because of the low dielectric constant of aluminum oxide, which increases the EOT. Furthermore, the excessive incorporation of Al degrades the carrier mobility in the channel.

Capping with an aluminum-containing material, such as Al_2O_3 or Al, has been studied for low power applications because it is simple and compatible with current integration techniques. Therefore, an analysis of the performance and reliability of pMOSFETs with Al_2O_3 or Al capping layers is necessary. This study compared the electrical and physical characteristics of pMOSFETs with Al_2O_3 or Al capping layers.

2. Experiment

pMOSFETs were fabricated using conventional CMOS process flow. A 2 nm HfO_2 film was deposited by atomic layer deposition (ALD) followed by a post-deposition annealing at 700 °C for 1 min in NH_3. Either 1 nm Al_2O_3 was deposited by ALD or 1 nm Al was deposited by physical vapor deposition. A 2 nm HfO_2-only dielectric was used as the control.

10 nm TiSiN metal gates were deposited by chemical vapor deposition followed by a poly-silicon capping layer for the silicide process. Spike annealing at 1070 °C was performed for source/drain activation. After the back-end process was completed, forming gas annealing was performed at 450 °C. The capacitance-voltage characteristics were measured at 100 kHz with Agilent E4980A. The equivalent

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oxide thickness (EOT) was simulated using the North Carolina State University CVC program with a quantum mechanical effect correction [23].

The depth profiles of Al atoms within the gate dielectrics of the samples were examined in 200 keV using a JEOL JEM-2100 F (Japan Electron Ltd., Tokyo, Japan) equipped with energy dispersive spectrometer (EDS). Each spectra were acquired with 1 Å beam size in scanning transmission electron microscopy (STEM) mode.

A charge pumping technique [24] was implemented to extract the trap densities (N_{it}) at the interface, which were correlated with the degree of carrier mobility.

3. Results and discussion

The high angle annular dark field (HAADF) STEM images showed no discrete Al_2O_3 or Al layers on top of the HfO_2 dielectrics after device fabrication (Fig. 1(a) and (c)). Both dielectrics were of similar physical thickness, despite the different levels of Al incorporation. Fig. 1 (b) and (d) show the depth profiles of Al atoms in the gate stacks. The Al-capped sample had a high level of Al incorporation in the dielectric, which was attributed to the relatively high number of Al atoms and lower binding energy of Al metal in the capping layer. Interestingly, the Al_2O_3-capped sample had a higher concentration of Al atoms at the interface of the dielectric and Si substrate than in the dielectric itself. The incorporation of Al atoms in the dielectric was confirmed by the capacitance. The EOTs of the control, Al_2O_3-capped and Al-capped samples were 8.4 Å, 9.6 Å and 11.3 Å, respectively. The EOT of the sample with Al capping was highest because more Al incorporation in the dielectric decreases the dielectric constant.

The flatband voltages (V_{FB}) have been reported to be shifted positively by Al incorporation in the gate stack. On the other hand, the V_{FB} shifts of both capped samples were similar despite the different total amounts of Al incorporation (0.37 V, 0.5 V, and 0.52 V for the control, Al_2O_3-capped and Al-capped, respectively), indicating that dipole formation at the interface was saturated.

Fig. 2 shows the effective channel mobility of each sample. Although both capped samples had a degraded effective carrier mobility compared to the control, Al_2O_3 capping had a lesser effect than Al capping. Therefore, the degradation of carrier mobility is related to

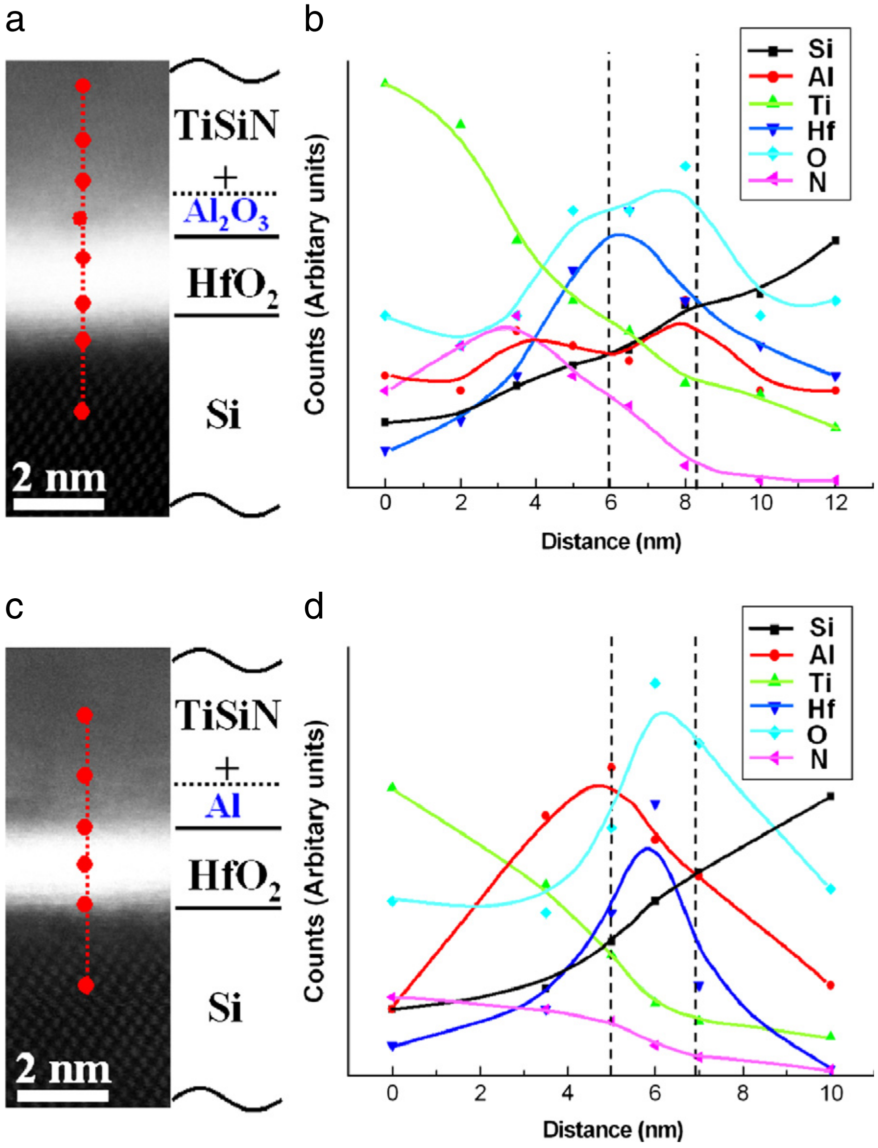

Fig. 1. Depth profiles of various atoms in the gate stacks with (a) Al_2O_3 and (b) Al capping layers. (HAADF-STEM images and EDS spectrum intensity profiles of various atoms in gate stacks with (a and b) Al_2O_3 (c and d) Al capping layers).

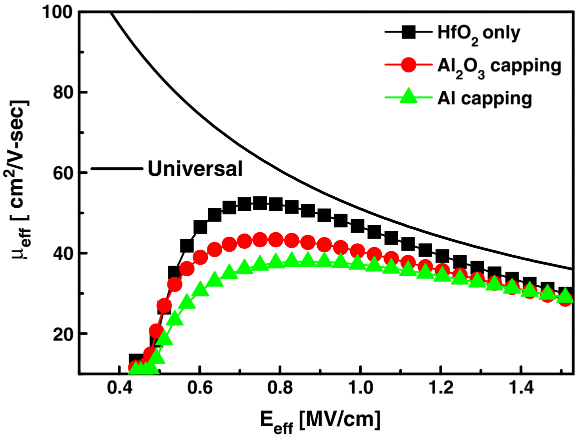

Fig. 2. Effective channel mobility of the control, Al_2O_3-capped and Al-capped samples.

the total amount of Al incorporated in the interface and dielectric rather than the dipoles, which are represented by the V_{FB} shifts.

Fig. 3 shows the trap densities (N_{it}) at the interface, which were extracted using charge pumping technique [24]. Since a lower frequency pulse during the charge pumping measurements allows more time to probe the deeper traps, the *x*-axis of Fig. 3 represents the physical distance from the interface of the channel and dielectric. The incorporation of Al atoms appears to be responsible for the increase in charge trap density because both capped samples had higher trap densities than the control. In particular, the Al-capped sample exhibited a rapid increase in trap density with distance into the dielectric, corresponding to the increase in Al concentration shown in Fig. 1. The increase in the number of charge traps at the interface resulted in a decrease in the effective channel mobility.

Negative-bias temperature instability (NBTI) was monitored to evaluate the effects of the capping layers on the reliability. Fig. 4 shows the NBTI characteristics of each sample under the same stress bias, $V_g - V_{th} = 1.2$ V, at 125 °C. The inset in Fig. 4 presents the V_{th} shifts (ΔV_{th}) after 1,000-sec stress as a function of the stress bias (V_g–V_{th}). The V_{th} shifts of the capped samples were higher than that of the control, indicating that the trap energy can be changed by incorporating Al. On the other hand, despite the different Al profiles of the Al and Al_2O_3 capped samples, their NBTI characteristics were similar. The NBTI of p-type MOSFETs with high-*k* dielectrics is strongly affected by charge trapping in the bulk traps in the dielectric [25,26]. This indicates that this difference in Al incorporation does not change the bulk charge trapping characteristics significantly [27]. A slight degradation of capped samples from the control sample can be attributed to the high trap density in bulk high-k and poorer interface quality due to Al diffusion.

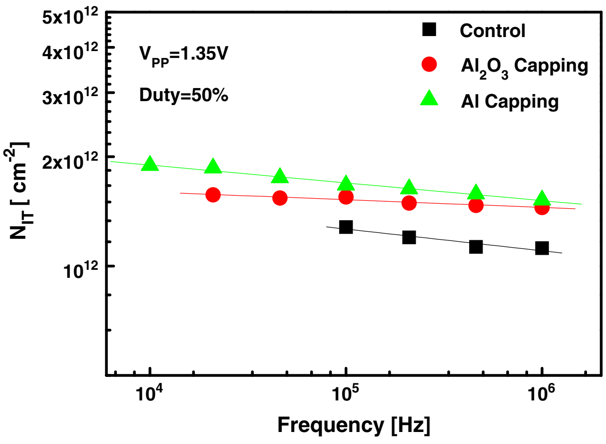

Fig. 3. Trap densities (N_{it}) in the interface layer extracted using the charge pumping technique.

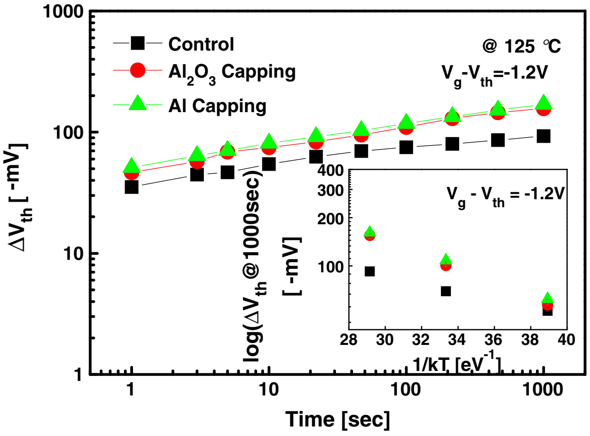

Fig. 4. Negative-bias temperature instability characteristics of the control, Al_2O_3-capped or Al-capped samples at $V_g - V_{th} = 1.2$ V. The inset shows the temperature dependence of the NBTI characteristics.

4. Conclusion

The effects of Al incorporation on V_{FB} modulation and the reliability of pMOSFETs were examined. The V_{FB} of pMOSFETs with either Al_2O_3 or Al capping could be modulated by dipole formation through Al diffusion into the interface layer. The magnitude of the V_{FB} shift was not proportional to the total amount of Al incorporated in the dielectric. Excessive incorporation of Al in the dielectric resulted in an increase in traps and degradation of the channel mobility. On the other hand, the NBTI characteristics of both the Al_2O_3 capping and Al capping samples were similar. The pMOSFET with Al_2O_3 capping showed superior V_{th} modulation, EOT reduction and carrier mobility compared to the Al-capped sample.

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